

Application No: 10/027,911

PATENT

In the Claims:

Please amend the claims as indicated:

31
1. (Cancel)2. (Amended) ~~The An~~ apparatus of claim 1, further comprising:

a first conductivity type junction formed between a first region of a first conductivity type and a second region of a second conductivity type;

a second conductivity type junction formed between the second region and a third region of the first conductivity type;

a third conductivity type junction formed between the third region and a fourth region of the second conductivity type, wherein the first, second and third conductivity type junctions are associated with a thyristor;

a low voltage trigger control coupled to the second region and the third region to provide a thyristor triggering current;

a first voltage reference node coupled to the first conductivity type junction; and

a second voltage reference node adapted to be isolated from the first voltage reference node during normal operating conditions, coupled to the fourth conductivity type junction to provide a current path between the first voltage reference node and the second voltage reference node during an electrostatic event, wherein the first voltage reference node and the second voltage reference node are to provide a common voltage reference.

Application No: 10/027,911

PATENT

- B'
3. (Original) The apparatus of claim 2, wherein the first voltage reference node and the second voltage reference node are ground nodes.
4. (Amended) The apparatus of claim ~~1~~2, wherein a capacitance between the first region and the fourth region is less than 120 femtofarads.
5. (Canceled)
6. (Canceled)
7. (Amended) The apparatus of claim ~~1~~2, wherein the low voltage trigger includes a zener diode.
- 112 {
8. (Original) The apparatus of claim 7, further comprising:
a first voltage reference node coupled to the first the first conductivity type junction;
a second voltage reference node adapted to be isolated from the first voltage reference node during normal operating conditions, coupled to the fourth conductivity type junction to provide a current path between the first voltage reference node and the second voltage reference node during an electrostatic event.
9. (Original) The apparatus of claim 7, wherein the zener diode includes a fifth region of the first conductivity type formed at least partially overlying the third region, and the fifth region has a different amount of doping than the third region.
10. (Original) The apparatus of claim 9, wherein the zener diode further includes a sixth region of the second conductivity type formed overlying the fifth region and the second region
- C
11. (Amended) The apparatus of claim ~~1~~2, wherein the low voltage trigger includes a field effect transistor.
- C
12. (Original) The apparatus of claim 11, wherein the field effect transistor includes a first current node coupled to the second region, a second current node coupled to the fourth region, and a control node coupled to the second region.
13. (Original) The apparatus of claim 11, further comprising:
a first voltage reference node coupled to the first conductivity type junction; and
- 112

Application No: 10/027,911

PATENT

B¹
112
a second voltage reference node adapted to be isolated from the first voltage reference node during normal operating conditions, coupled to the fourth conductivity type junction to provide a current path between the first voltage reference node and the second voltage reference node during an electrostatic event.

14. (Original) The apparatus of claim 13, wherein the control node includes a gate structure formed over a portion of the third region.
15. (Original) The apparatus of claim 14, wherein the first node is connected to a fifth region of the second conductivity type formed overlying the second region and the third region.
16. (Original) The apparatus of claim ¹⁵14, wherein the gate structure is formed over an area between the fifth region and the fourth region.
17. (Amended) The apparatus of claim 1-2 wherein the apparatus is formed using a complimentary metal oxide semiconductor process.
18. (Original) A thyristor formed in an integrated data processing device, the thyristor comprising:
a first conductivity type junction formed between a first region of a first conductivity type and a second region of a second conductivity type;
a second conductivity type junction formed between the second region and a third region of the first conductivity type;
a third conductivity type junction formed between the third region and a fourth region of the second conductivity type; and
an anode node connected to one or more regions including the first region, wherein each of the one or more regions connected to the anode node are of a common connectivity type. 12
19. (Original) The thyristor of claim 18 further comprising:
a low voltage trigger control portion coupled to the second region and the third region to provide a thyristor triggering current at a voltage of less than 10 volts.

Application No: 10/027,911

PATENT

20. (Original) The thyristor of claim 18 formed using a complimentary metal oxide semiconductor process.
21. (Original) An apparatus comprising:
a first voltage reference node to provide a first voltage reference;
a second voltage reference node, adapted to be isolated from the first voltage reference node during normal operating conditions, to provide the first voltage reference;
a thyristor coupled between the first voltage reference node and the second voltage reference node to provide a current path between the first voltage reference node and the second voltage reference node during an electrostatic event.
22. (Previously Amended) The apparatus of claim 21 further comprising:
a first circuit connected to the first voltage reference node; and
a second circuit connected to the second voltage reference node.
23. (Previously Amended) The apparatus of claim 22 wherein the first circuit is an analog circuit and the second circuit is a digital circuit.
24. (Previously Amended) The apparatus of claim 22 wherein the first circuit is a radio frequency analog circuit.
25. (Previously Amended) The apparatus of claim 23 wherein the second circuit is a digital circuit.
26. (Previously Amended) The apparatus of claim 24 wherein the second circuit is an analog circuit.
27. (Amended) A method comprising the steps of:
detecting a voltage difference between a first voltage reference node and a second voltage reference node to determine when an electrostatic discharge event is occurring,
wherein, the first voltage reference node and the second voltage reference node are isolated from each other and are to provide a first voltage reference ;
providing conductive path through a ~~thyristor~~ thyristor when the voltage difference is less than approximately 10 volts.

Application No: 10/027,911

PATENT

B¹ 28. (Previously Amended) The method of claim 27, wherein the first voltage reference node and the second voltage reference node are at a common potential during a normal mode of operation.

B¹ 29. (New) The method of claim 2, wherein triggering current occurs at a voltage of less than 10 volts.

30. (New) An apparatus comprising:

a thyristor comprising a first p-doped region, a first n-doped region, a second p-doped region, and a second n-doped region, a first junction formed by the first p-doped and first n-doped region, a second junction formed by the first n-doped region and the second p-doped region, and a third junction formed by the second p-doped region and the second n-doped region, an anode coupled to the first n-doped region only through the first p-doped region, and a cathode coupled to the second p-well only through the second n-doped region; and

a first voltage reference node coupled to the anode, and

a second voltage reference node adapted to be isolated from the first voltage reference node during normal operating conditions coupled to the cathode

31. (New) The apparatus of claim 30, wherein the first voltage reference node and the second voltage reference node are to provide a common voltage reference.

32. (New) The apparatus of claim ³¹30, wherein the common voltage references is a ground voltage reference.

2 112
